(19) (11) Publication number: **58192154 A**

Generated Document.

PATENT ABSTRACTS OF JAPAN

(21) Application number: **57075376**

(22) Application date: **07.05.82**

(51) Intl. Cl.: **G06F 13/00** G11C 7/00

(30) Priority:

(43) Date of application publication: **09.11.83**

(84) Designated contracting states:

(71) Applicant: **CASIO COMPUT CO LTD**

(72) Inventor: **FUJISAWA HIDETAKA**

(74) Representative:

(54) MEMORY DEVICE HAVING AUTOMATIC DATA PROCESSING FUNCTION

(57) Abstract:

PURPOSE: To attain the parallel processing together with a CPU, by decoding an instruction code transmitted from the CPU, designating the address of a memory device sequentially, and eliminating increment of the number of connecting lines with the CPU even if the storage capacity is increased.

CONSTITUTION: An instruction code among data D1WD4 transmitted from the CPU is decoded at a decoder 6b, transmitted to a timing generating circuit 6a, and control instructions O1WO7 are outputted. An address of an RAM20 is designated accoding to the control instructions O1WO7. Thus, even if the capacity of the RAM20 is increased, the number of bus lines connected to the CPU is not increased. Further, the movement of data in the RAM20 and the search of data are processed automatically independently of the CPU. Then, the CPU performs other processings in parallel.